

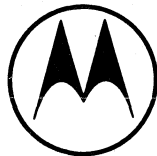
AN-751

Application Note

A DISASSOCIATED INTERCARRIER TELEVISION VIDEO IF AMPLIFIER

Prepared by:
S. James Reid
Applications Engineering

This application note discusses a unique video IF system, incorporating the MC1331, low-level multiplier detector. Problem areas in IF design are discussed and the specific solutions are shown.



MOTOROLA Semiconductor Products Inc.

A DISASSOCIATED INTERCARRIER TELEVISION VIDEO IF AMPLIFIER

INTRODUCTION

Video IF systems have seen little change in design goals since the concept of intercarrier sound amplification in TV receivers was adopted. The introduction of color and the suppressed subcarrier chroma channel uncovered an undesirable beat product between the chroma and the intercarrier sound. This began the compromise of sufficient 41.25 MHz trapping versus good, noise-free audio performance. It is apparent that demodulation of both picture information and sound IF carriers in a common diode is not possible. Low level ("exalted carrier") detectors promised relief from this need for separate detectors, as they are cleaner detectors, with lower harmonic outputs. Another compromise becomes apparent, however, in these low level detectors. If the detector L-C tuned circuit Q is kept high, excellent beat rejection is achieved, but the system fine tuning becomes too critical due to phase distortions in the detector. Low tank Q, on the other hand, leaves the unsatisfactory beat product situation. Attempts at complex tank circuits, while improving the beat product rejection, have not eliminated the critical tuning associated with detector phase distortions.

The complete separation of the 41.25 MHz intercarrier and the video information is necessary for optimum high performance in the TV receiver. The introduction of the

MC1331, video IF low-level detector has opened a new level of performance to the TV set manufacturer.

The circuit described will exhibit positive performance in all areas, without any of the compromises previously found necessary in IF design. This is possible because of the addition of the separate low-level multiplier detector, which still uses the associated video carrier for demodulation of the 41.25 MHz sound inter-carrier to the 4.5 MHz sound IF carrier. This allows the separation of the sound intercarrier from the video information at the IF input, before any shaping or trapping network can introduce power loss at the 41.25 MHz frequency, which deteriorates the sound intercarrier signal-to-noise (see Figure 1).

There is no power loss ahead of the amplifier, and because it can be made narrow-band, a single device can provide sufficient gain for clean detection in the MC1331. The receiver, 30 dB audio quieting, with this video IF system, is well below 10 μ V antenna signal strength. This is sound performance that is competitive with any TV receiver now produced. This performance is not achieved at the expense of 920 kHz beat rejection, which is the only alternative available to the IF designer. An additional benefit of the separate detector is the elimination of the sound buzz present with heavy modulation

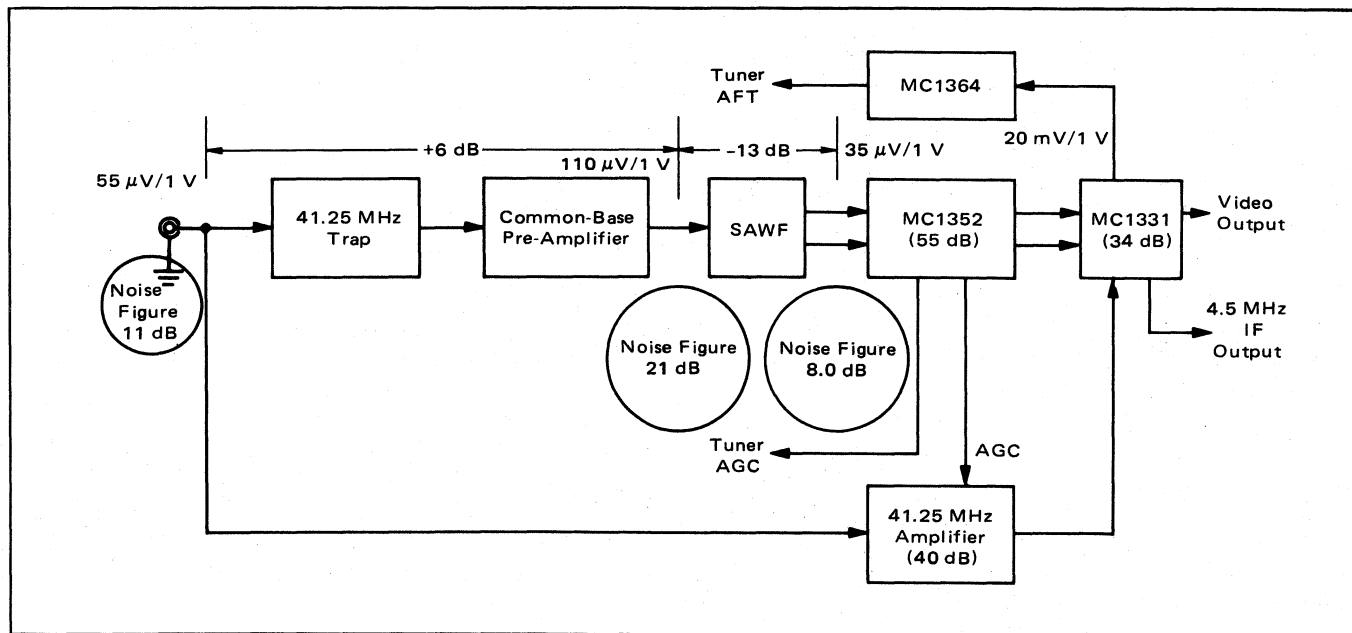


FIGURE 1 – System Block Diagram

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

of "white lettering" superimposed on normal video information. Anything less than complete overmodulation (eliminating the 45.75 MHz carrier) does not introduce "white lettering buzz".

The IF system shown in Figure 1, exhibits the partitioning of IF gain that maintains small, integrated circuit chip size, with the inherent lower replacement cost for failed devices and the higher manufacturing device yield with associated lower piece-part cost. The common-base amplifier is used to provide tuner-IF isolation, and to improve the IF noise figure. The acoustic surface wave filter provides the video IF bandpass shaping. The MC1352 was chosen to exhibit a device available for use in TV partitioning that does not include a form of "jungle" circuit. The MC1349 or a similar device, could be used for those partitionings that include an integrated AGC function. An MPS-H32 is used as the intercarrier sound amplifier, with its AGC characteristic tracking the MC1352. To complete the IF system, the MC1364 performs the AFT function.

CIRCUIT DESCRIPTION MC1331

This integrated circuit is a second generation, balanced multiplier, low-level detector. Although the early low-level detectors had improved the system performance with regard to gain, linearity and the elimination of complicated circuit shielding by reduced RF levels, compared to discrete detector systems, certain problems remained:¹

- 1) The compromise between sound sensitivity and the 920 kHz beat product.
- 2) The AGC set up problems due to wide zero signal dc output ranges and to the lack of adequate supply variation rejection.
- 3) A developing demand for further improvements in linearity in the form of better differential gain and phase.
- 4) Overload performance that allowed undesired detector output causing AGC lockout.

The solution of these problem areas was of prime concern in the design of the MC1331. A brief description of the circuit operation will point out some specific solutions.

Basic Video Detector

The operation of multiplier detectors has been covered before. 1, 2, 3 Equation (1), describing the detected video output term, is useful in describing the circuit operation and specific idiosyncrasies.

$$v_o = A_o \cos \omega_m t \cos \phi \quad (1)$$

The $A_o \cos \omega_m t$ represents the modulation information at the multiplier output. The $\cos \phi$ term represents the contribution of the carrier phase difference between the linear amplifier and the switching amplifier as shown in Figure 2. The switching differential amplifier is comprised of devices Q11 and Q12. The transistors Q9 and Q10 are the linear differential amplifier. Transistors Q1 and Q2, buffer the

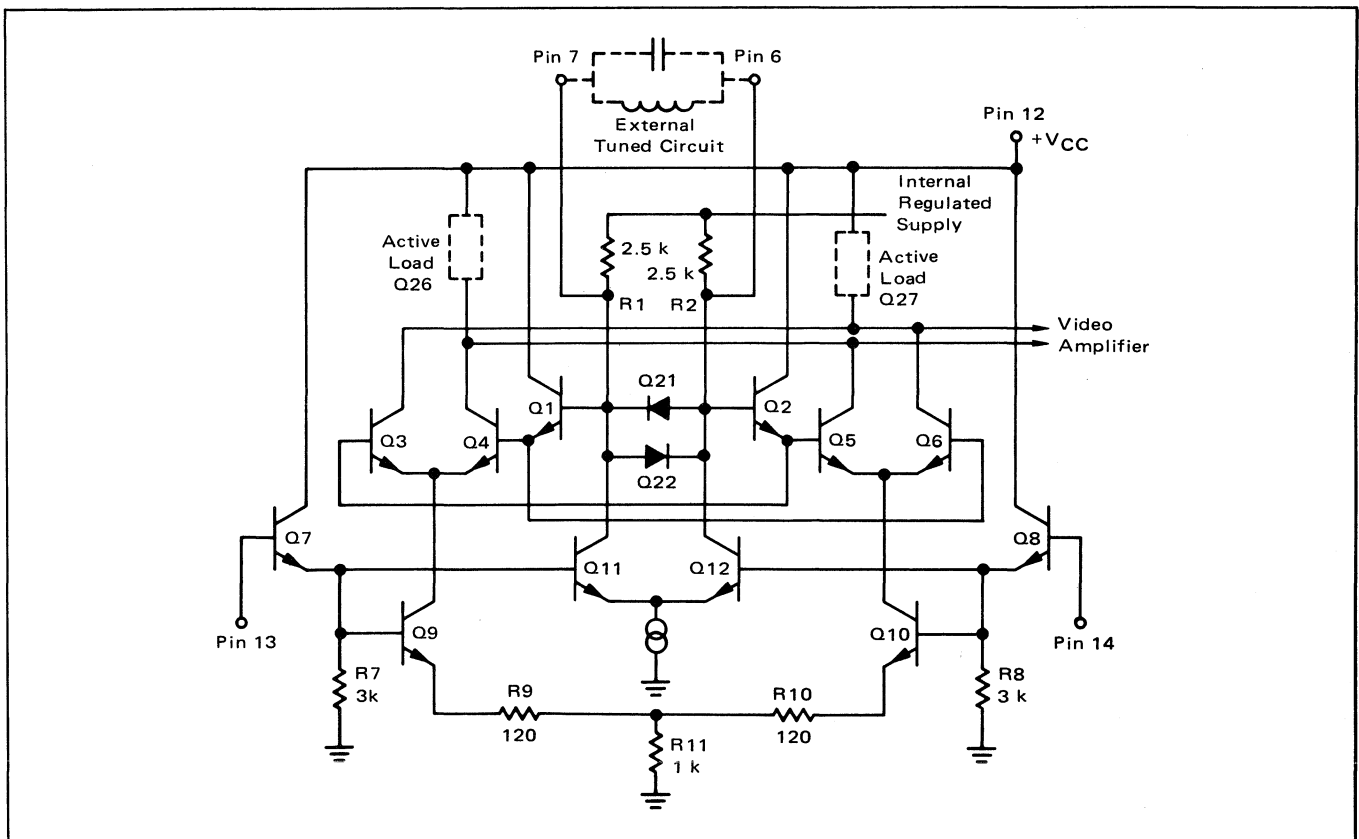


FIGURE 2 - Basic Multiplier Detector Circuit

switching amplifier drive to the quad detector, Q3, Q4, Q5 and Q6, which is driven directly from the linear amplifier. The tuned L-C circuit adjusts the phase difference between the switching channel and the linear channel to 0° or 180° for optimum detection, see Equation (1).

The diodes, Q21 and Q22, limit the phase shift in the switching channel, preventing excessive differential gain (typically less than 5%).¹ An unbalance in the quad detector, V_{BE} offset, can cause a dc offset of the detector at zero-signal input. As input signal is increased, removal of the offsets causes perturbations of the video detector transfer function. By keeping the gain of the switching channel high, > 15 , these signal inversions can be kept to low input signal levels, corresponding to modulation depths greater than the 87.5% white level.

The Q of the L-C circuit across Pins 6 and 7 must be chosen with two opposing factors in mind, the ease of

fine tuning versus the beat production. This system design incorporates a deep 41.25 MHz trap in the video channel, with a low Q tank circuit being used for less critical fine tuning, without a loss in the 920 kHz beat product rejection.

The excellent circuit linearity is noted in the transfer function shown in Figure 3. The conversion gain of 34 dB, gives adequate sensitivity to the detector and the high, linear p-p output reserve swing reflects the superb detector efficiency. This linearity contributes to the low overall differential gain and phase.

Sound Detector

The separate sound detector eliminates the compromise of sound sensitivity and 920 kHz beat. The switching signal developed in the video detector is used for demodulation of the 41.25 MHz intercarrier sound to the 4.5 MHz

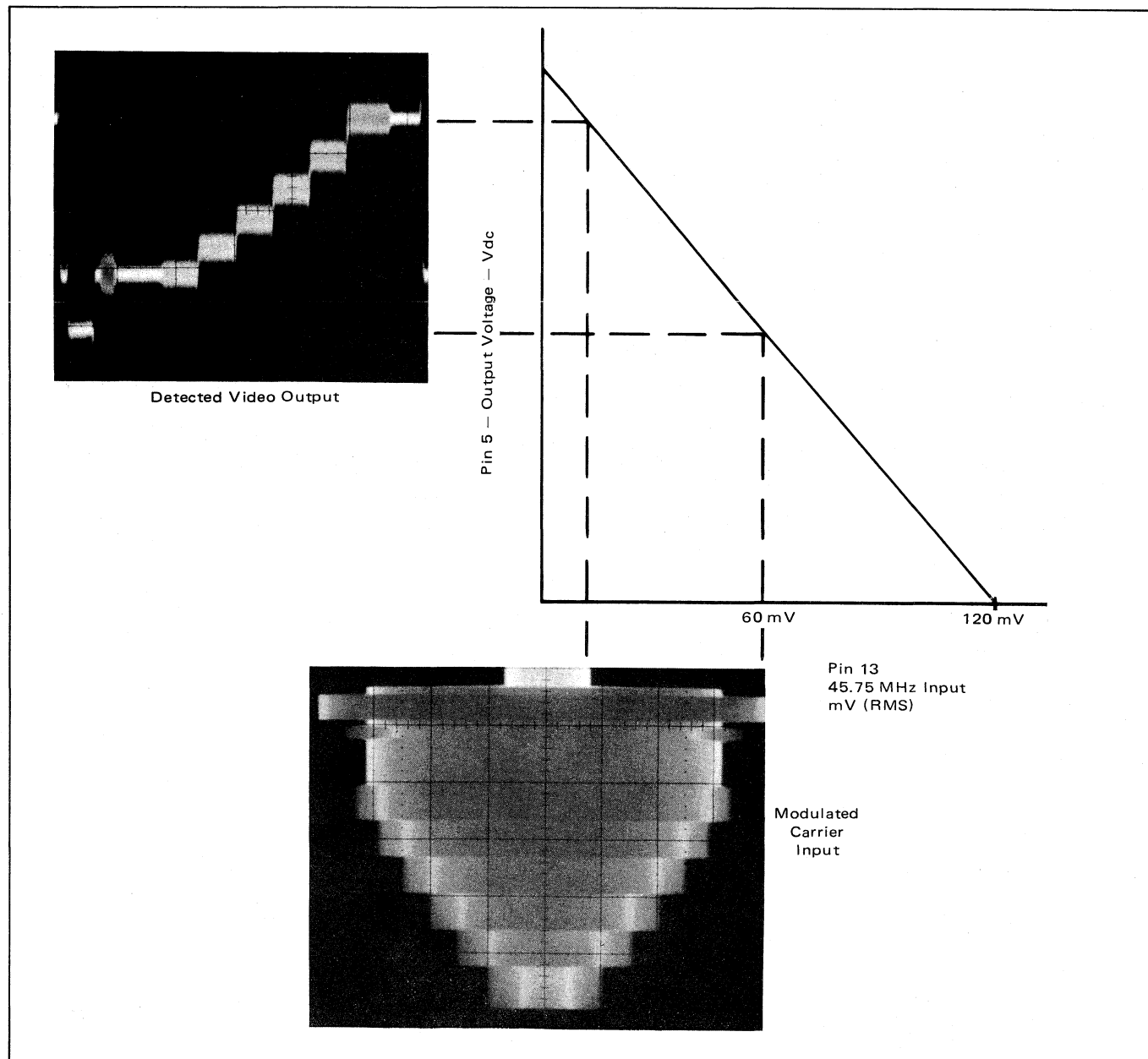


FIGURE 3 - Transfer Curve

sound IF carrier. The switching signal is coupled into the detector via Q17, (see Figure 4). The signal drives the simple differential amplifier detector Q15 and Q16. The tuned circuit at Pin 10 is tuned to 4.5 MHz and effectively establishes the detector bandwidth of ± 200 kHz (see Figure 5). The detector circuit output is buffered by Q19 emitter follower, providing a low impedance drive for the sound IF. The input to the detector is also buffered by Q13, providing the desired high input impedance. The conversion gain of the detector is 20 dB, with outputs to 100 millivolts easily available.

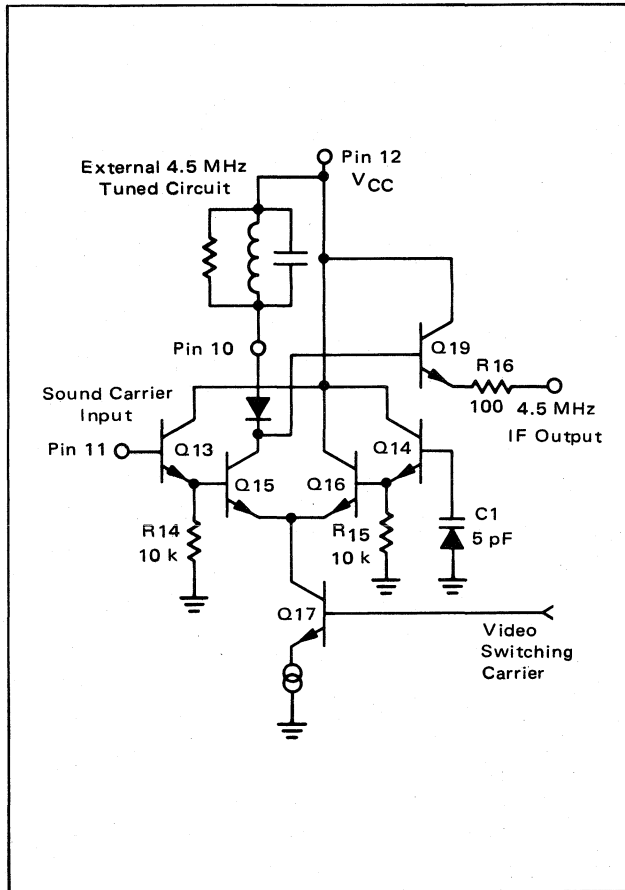


FIGURE 4 – Sound Detector

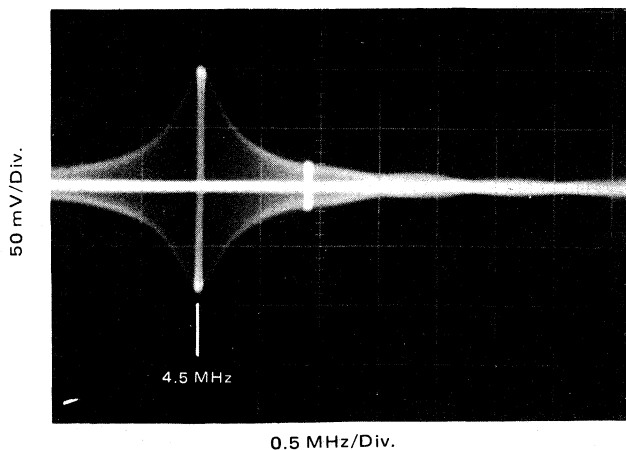


FIGURE 5 – Sound Channel Output

Video Amplifier

The video amplifier in Figure 6 completes the improvement in differential phase and gain, by eliminating the lateral PNP device from the video amplifier that contributes to linearity problems. The detector differential output currents are combined in a “full-wave” output, with greater dc stability and less power supply dependence. The detected signal currents from the multiplier are combined in transistor Q41. Q38 and Q40 invert one of the differential currents before summing. The signal current is then inverted to a negative video output voltage in R36 (4.5 k) which is operating from a zener regulated supply. This gives the output voltage a supply rejection of 20 dB. The output is buffered by Q49 and Q50.

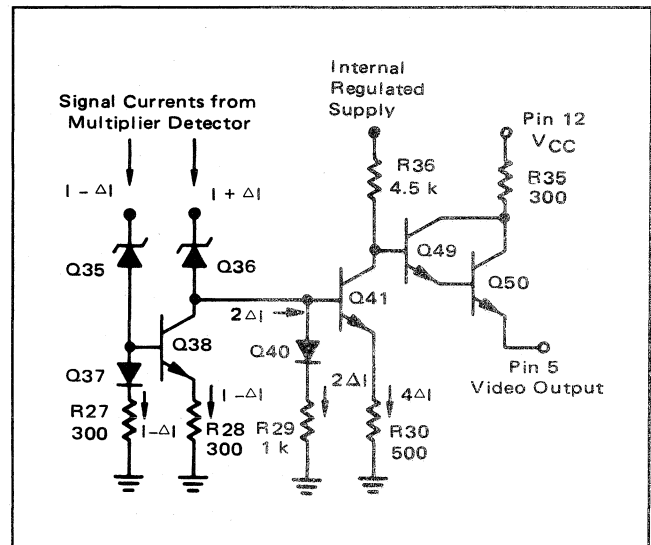


FIGURE 6 – Video Amplifier

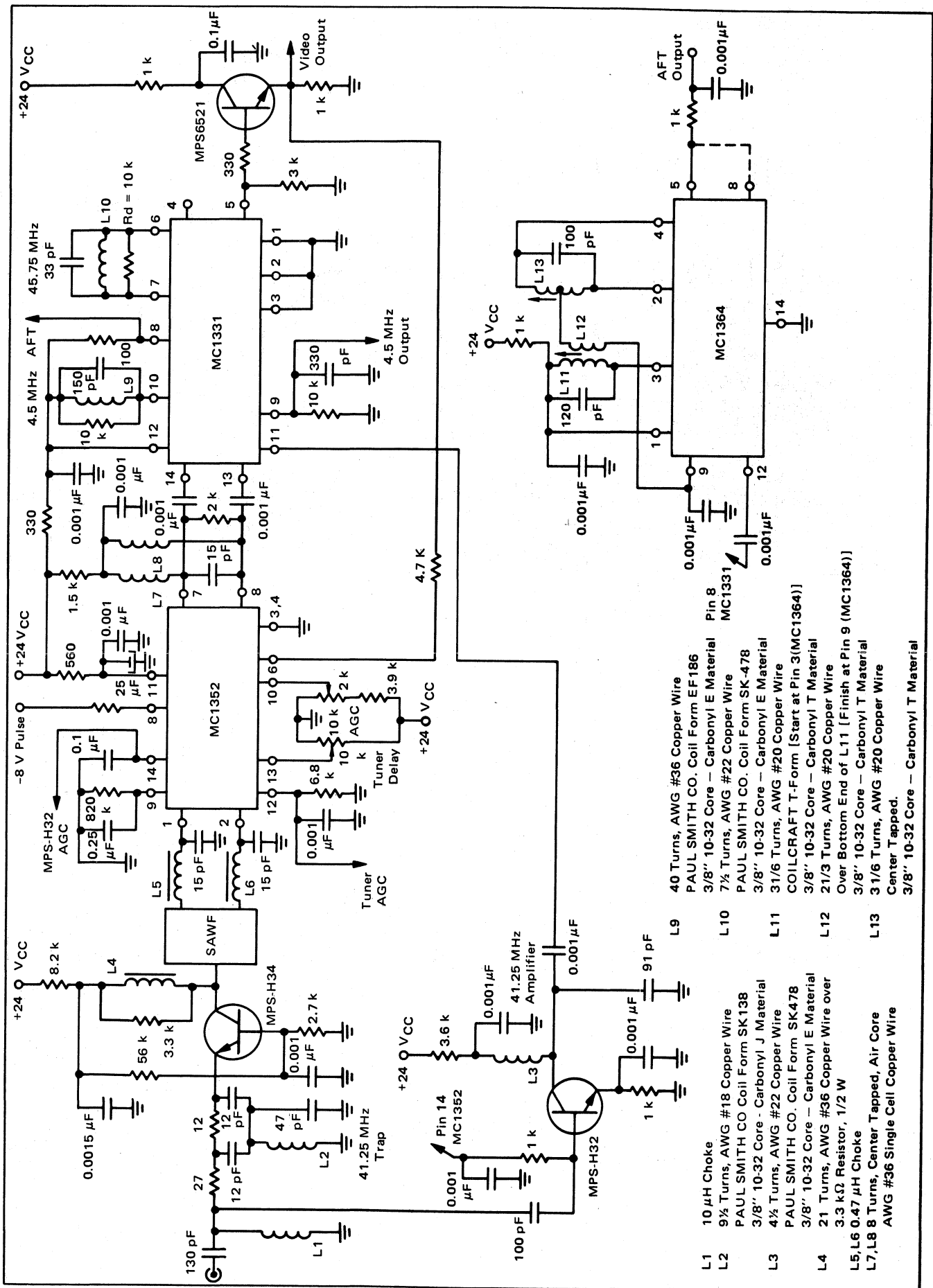
Overload Protection

The elimination of possible AGC lockout is due to the overload sensing and clamping devices Q43, Q39 and Q56 as shown in Figure 7. High signal levels into the input Pins 13 or 14 are detected and clamp Q49 base at ground, thus preventing an output signal “reversal”. This clamping occurs at input signal levels well above 150 mV(rms), thus not interfering with normal operation (see Figure 3).

MC1352

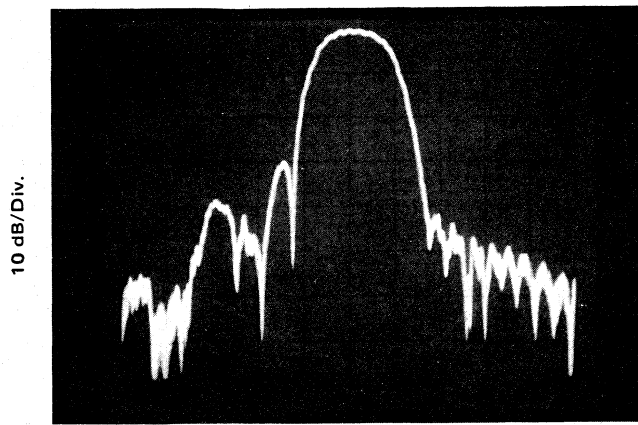
The major portion of the gain of this IF system is developed by the amplifier section of the MC1352. This device also develops the keyed AGC for the IF and the delayed AGC for the tuner. The circuit operation has been described in other articles 4, 5 and will not be repeated here. The circuit board layout, Figure 15, was developed to keep ground copper around the MC1352 and to reduce any tendency for regeneration. Extra jumpers were used with this in mind.

The interstage matching between the MC1352 and the MC1331 has been simplified due to the input filter, which has the total system band shape requirements. Therefore, the interstage needs to be broadband and may be fixed

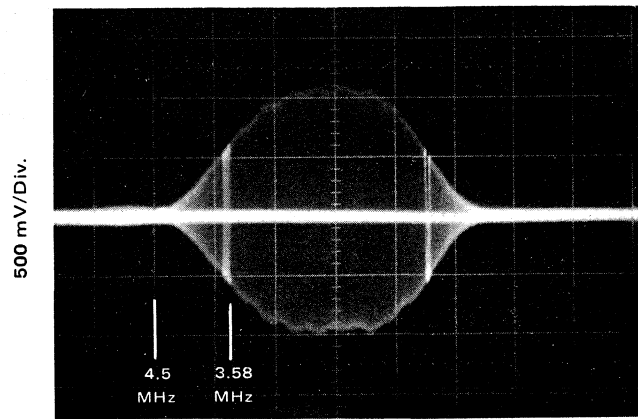


- L1 10 μH Choke
- L2 9 1/2 Turns, AWG #18 Copper Wire
- L3 PAUL SMITH CO Coil Form SK138
- L4 3/8" 10-32 Core - Carbonsyl J Material
- L5 4 1/2 Turns, AWG #22 Copper Wire
- L6 PAUL SMITH CO. Coil Form SK478
- L7 3/8" 10-32 Core - Carbonsyl E Material
- L8 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W
- L9 10 μH Choke
- L10 9 1/2 Turns, AWG #18 Copper Wire
- L11 PAUL SMITH CO Coil Form SK138
- L12 3/8" 10-32 Core - Carbonsyl J Material
- L13 PAUL SMITH CO. Coil Form SK478
- L14 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W
- L15 4 1/2 Turns, AWG #22 Copper Wire
- L16 PAUL SMITH CO. Coil Form SK478
- L17 3/8" 10-32 Core - Carbonsyl E Material
- L18 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W
- L19 10 μH Choke
- L20 9 1/2 Turns, AWG #18 Copper Wire
- L21 PAUL SMITH CO Coil Form SK138
- L22 3/8" 10-32 Core - Carbonsyl J Material
- L23 4 1/2 Turns, AWG #22 Copper Wire
- L24 PAUL SMITH CO. Coil Form SK478
- L25 3/8" 10-32 Core - Carbonsyl E Material
- L26 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W
- L27 9 1/2 Turns, AWG #18 Copper Wire
- L28 PAUL SMITH CO Coil Form SK138
- L29 3/8" 10-32 Core - Carbonsyl J Material
- L30 4 1/2 Turns, AWG #22 Copper Wire
- L31 PAUL SMITH CO. Coil Form SK478
- L32 3/8" 10-32 Core - Carbonsyl E Material
- L33 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W
- L34 9 1/2 Turns, AWG #18 Copper Wire
- L35 PAUL SMITH CO Coil Form SK138
- L36 3/8" 10-32 Core - Carbonsyl J Material
- L37 4 1/2 Turns, AWG #22 Copper Wire
- L38 PAUL SMITH CO. Coil Form SK478
- L39 3/8" 10-32 Core - Carbonsyl E Material
- L40 21 Turns, AWG #36 Copper Wire over 3.3 kΩ Resistor, 1/2 W

FIGURE 8 - Complete Video IF Schematic



2.0 MHz/Div.
FIGURE 9 – SAWF Response Curve



1.0 MHz/Div.
FIGURE 10 – Video Channel Output

Input Network

The IF input cable is terminated by the 130 pF capacitance, the 10 μ H choke and the input of the common-base amplifier stage. The 41.25 MHz trap in the emitter circuit introduces over 30 dB of attenuation at the sound inter-carrier frequency in the video channel (Figure 12). The 27 Ω resistor isolates the trapping from the 41.25 MHz take off.

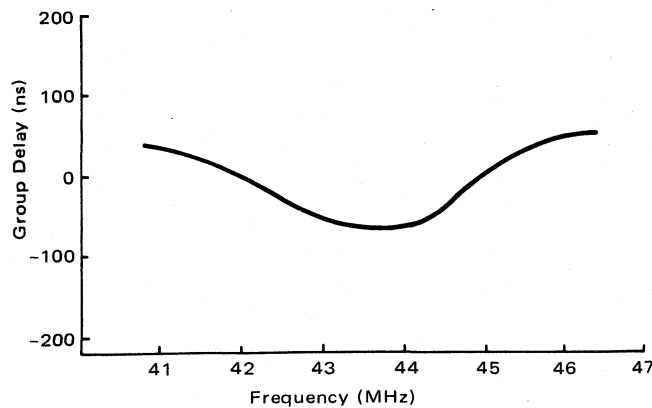
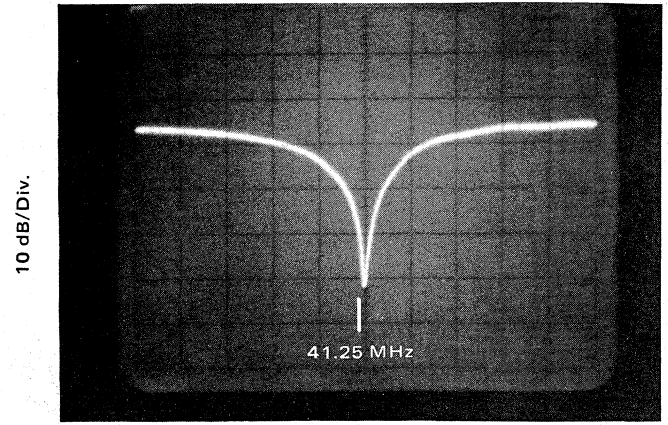


FIGURE 11 – SAWF Group Delay



500 kHz/Div.
FIGURE 12 – 41.25 MHz Trap

41.25 MHz Amplifier

The MPS-H32, forward gain reduction transistor is used as the separate sound channel amplifier. The tracking of the AGC to the MC1352 is accomplished by choosing the emitter resistor value that will force the MPS-H32 to maximum gain at the MC1352 maximum gain voltage. The 40 dB gain reduction is made to coincide by selection of a collector resistance, which will reduce the V_{CE} on the transistor causing 40 dB gain reduction. A small amount of mistracking will not create any problems, since the system has sufficient dynamic range. The circuit Q has not been made high, to prevent any problems associated with fine tuning, although the increasing Q of the stage at maximum gain reduces the noise bandwidth (Figures 13 and 14).

MC1364

The automatic fine tuning function is handled by the MC1364 integrated circuit. Since the MC1364 is a well known device, no circuit description will be given. The input was not tuned, as MC1331 provides a low impedance source and an AM rejection of 30 dB typical. The circuit board layout should be followed as the coils have mutual coupling needed to establish the tight S curve.

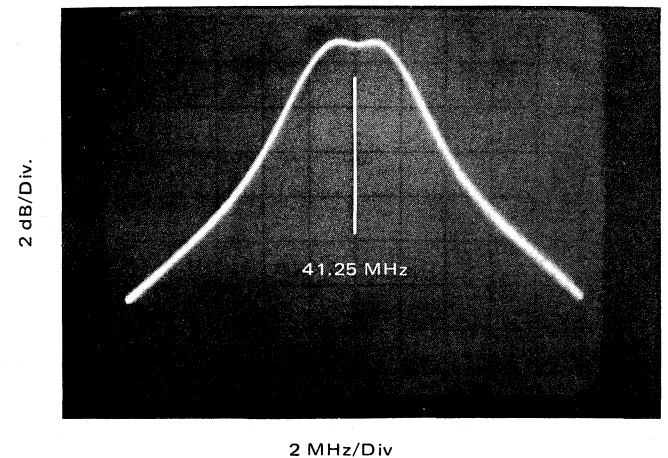


FIGURE 13 – 41.25 MHz Amplifier – 40 dB Gain Reduction

2 dB/Div.

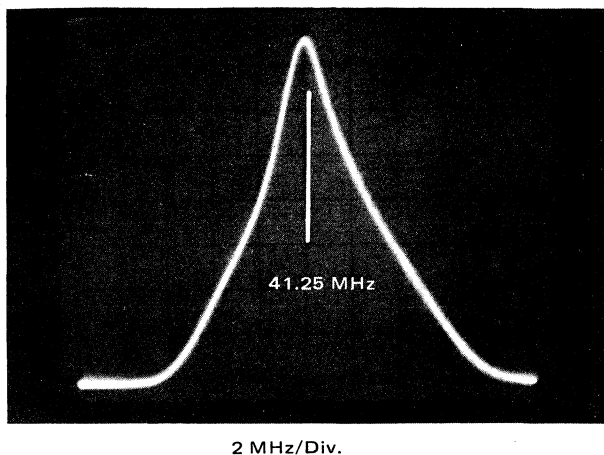


FIGURE 14 — 41.25 MHz Amplifier Maximum Gain

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